REMARKS

Claims 1 through 7 are currently pending in the application.

This amendment is in response to the Office Action of March 8, 2004.

Preliminary Amendment

Applicants note the filing of a Preliminary Amendment on January 22, 2004, which filing was not acknowledged in the outstanding Office Action. Should the Preliminary Amendment have failed to have been entered in the Office file, Applicants will provide a true copy to the Examiner.

Double Patenting Rejection Based on U.S. Patent 6,600,335

Claims 1 through 7 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 through 7 of U.S. Patent 6,600,335. In order to avoid further expenses and time delay, Applicants elect to expedite the prosecution of the present application by filing a terminal disclaimer to obviate the double patenting rejections in compliance with 37 C.F.R. §1.321 (b) and (c). Applicants' filing of the terminal disclaimer should not be construed as acquiescence of the Examiner's double patenting or obviousness-type double patenting rejection. Attached is the terminal disclaimer and accompanying fee.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on Admitted Prior Art of Figs. 1 and 4 in view of Mennitt et al. (U.S. Patent 5,334,857)

Claims 1 through 7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Admitted Prior Art of Figs. 1 and 4 in view of Mennitt et al. (U.S. Patent 5,334,857). Applicants respectfully traverse this rejection, as hereinafter set forth.

Applicants further submit that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there

must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants have amended the claimed invention to clearly distinguish over the cited prior art.

The admitted prior art of FIGs. 1 through 4 of the specification teaches or suggests an exemplary chip package 10, typically comprised of an individual substrate 12 having an elongated aperture 14 extending through the middle of the substrate. The substrate may be a printed circuit board. A semiconductor die 16, such as a dynamic random access memory (DRAM) is mounted on the opposite (or bottom) side of the substrate. The semiconductor device 16 often has a plurality of bond pads 20 in single or multiple columns on active surface 18 of the semiconductor die 16. Active surface 18 can be seen through aperture 14. The substrate 12 has a top or upward facing surface 22 which also has a plurality of contact or bond pads 24 located along the periphery of aperture 14. Circuit traces 26 on or within the substrate 12 provide electrical connection to bond pads 20 which in turn are electrically connected to solder balls 28. Solder balls 28 are in electrical connection with or attached to a contact pad. The solder balls 28 may also be placed directly on top of the termination point of a circuit trace 26. The solder balls or conductive elements are arranged in a grid pattern and are of a carefully selected size and spacing, or pitch. The contact or bond pads 20 on active surface 18 of die 16 are electrically attached to contact pads 24 located on surface 18 of substrate 12 using wire bonding. The bond wires are shown as element 30. FIGs. 2 and 3 show cross-sectional views of the above-described structure. As shown in FIG. 2 semiconductor die 16 is attached to bottom side of substrate 32 using adhesive 34. FIG. 3 shows an encapsulant 38 disposed over contact pads 24, bond wires 30, and bond pads 20 for protection. FIG. 4 shows test tooling for use with the chip packages described in FIGs. 1 through 3. Each ball grid array (BGA) package 10 is placed in the chip receiving cell 44 of tray or holder 42. Chip 10 may be coated with encapsulant 38. Once chip 10 is properly seated in tray 42, probe head 46 is moved toward package 10 so as to contact each

probe 48 with a conductive element such as solder ball 28. Once the chip package 10 has been burned-in and tested, the probe head 46 is withdrawn and the chip package 10 is removed from tray or holder 42. At this point the chip package is ready for further processing, if the test has been successful.

Mennitt teaches or suggests a semiconductor device having test-only contacts to reduce the size of the device. (Abstract). After testing, the test-only contacts are removed, thus reducing the size of the device. The invention is particularly directed toward devices employing over-molded pad array carriers (OMPAC). (Col. 2, lines 57-60). A semiconductor device 10 includes a package substrate material 12, shown as a portion of a strip of material. (Col. 3, lines 1-2). The package substrate material 12 is in strip form to facilitate handling during automated manufacturing. Package substrate material 12 also has alignment holes 14 which are used to index the strip through manufacturing equipment. Device alignment holes 15 are used to align device 10 to the manufacturing equipment once the device has been separated from the strip. (Col. 3, lines 10-20). Conductive traces 16 are formed on the top surface of package substrate 12. Each conductive trace 16 electrically couples a terminal or bond pad 18 of semiconductor die 20 to an electrically conductive via 22. (Col. 3, lines 24-28). The conductive traces are electrically couples to the die by conductive wires 23. (Col. 3, lines 30-32). Device 10 also includes a package body 24 which encapsulates semiconductor die 20, wire bonds 23, portions of conductive traces 16, and portion of the top surface of package substrate 12. (Col. 3, lines 48-52). Each trace 16 formed on the top of package substrate 12 is routed to a solder ball 26 on the bottom of the package substrate by conductive vias 22. (Col. 3, lines 64-66). The solder balls of device 10 are the external electrical contacts used to access semiconductor die 20. When used, device 10 is mounted to a user substrate, such as a printed wiring board. The solder balls 26 correspond with the conductive pads or terminals on the user substrate. The solder balls 26 are reflowed and bonded to the pads, thus fixing the device to the substrate. (Col. 4, lines 18-26). External test contacts not needed by the user are removed. (Col. 4, lines 44-48).

Applicants respectfully submit that any combination of the admitted prior art and Mennitt under 35 U.S.C. § 103 fails to teach or suggest all the limitations of the presently claimed invention calling for "providing a burn-in and test fixture having a pattern of contacts having a

first predetermined pattern corresponding to a second pattern of contacts of an unrelated semiconductor die", "providing a plurality of ball grid array semiconductor packages connected to a substrate, each semiconductor package . . . a portion of the substrate having a first surface and a second surface opposite the first surface and having an aperture through the portion of the substrate in communication with the first and second surfaces thereof", "attaching a semiconductor device having an active surface with a plurality of bond pads thereon to one of the first and second surfaces of the substrate with the plurality of bond pads exposed within the aperture of the substrate", "forming a plurality of ball grid array connective elements on one of the first surface and the second surface of the portion of the substrate", "forming a plurality of test pads on a severable portion of the portion of the substrate, the plurality of test pads arranged in a first preselected pattern, the first preselected pattern of test pads having a predetermined pattern corresponding to the second pattern of contacts of the another unrelated semiconductor device for eliminating modification of the burn-in and test fixture for mating with a ball grid array semiconductor package", "forming a plurality of substrate bond pads on one of the first surface and the second surface of the portion of the substrate", "connecting selected bond pads of the plurality of bond pads on the active surface of the semiconductor device with selected substrate bond pads of the plurality of substrate bond pads using a plurality of bond wires extending therebetween", "providing a first plurality of circuit traces selectively connecting the selected substrate bond pads of the plurality of substrate bond pads with selected connective elements of the plurality of ball grid array connective elements", "providing a second plurality of circuit traces selectively connecting the selected connective elements of the plurality of ball grid array connective elements with selected test pads of the plurality of test pads", "placing the at least one ball grid array semiconductor package in a burn-in and test apparatus having a plurality of test probes", "contacting selected test probes of the plurality of test probes with the selected test pads of the plurality of test pads", "burning-in and testing the at least one ball grid array semiconductor package by applying and routing electrical energy to the selected test pads of the plurality of test pads by way of the selected test probes of the plurality of test probes", and "severing the portion of the substrate to form at least one ball grid array semiconductor package".

The prior art of FIGs. 1 through 4 does not teach or suggest test pads. While Mennitt teaches test pads, those pads are used only for manufacturer's final testing for a burn-in test fixture specifically designed for such test pads, not a test fixture designed for the pads of another semiconductor die. Additionally, Mennitt does not teach or suggest a second plurality of circuit traces that selectively connect to the test pads.

In contrast to any combination of the cite prior art, the preselected configuration of the test pads of Applicants' invention can be used for any semiconductor device. Burn-in and testing can be performed using existing tooling having test probes arranged in the same configuration as the test pads for previous semiconductor die having different test pad configurations. Thus, Applicants' invention eliminates the need for specific tooling for each test pad configuration. Applicants respectfully suggest that the motivation to combine the teachings of Mennitt with the prior art of FIGs. 1 through 4 must be based on impermissible hindsight and even if combined, do not result in the presently claimed invention by teaching or suggesting all the claim limitations of the presently claimed invention of independent claim 1.

As the proposed combination of the prior art of FIGs. 1 through 4 and Mennitt fails to teach or suggest every element of claim 1, the claim is not rendered obvious in view of the proposed combination under 35 U.S.C. § 103. Therefore, claim 1 is allowable.

Claims 2 through 7 are each allowable as depending, either directly or indirectly, from claim 1.

Claim 2 is further allowable as Mennitt or the admitted prior art does not teach or disclose that test pads can be arranged in a thin small outline package pin-out pattern. In fact, Mennitt teaches away from providing test pads in a thin small outline package pin-out pattern since the test pads are removed and are not used operationally. The test contacts are implemented in a form that the device manufacturer selects and may not be compatible with the user's equipment. Indeed, because the test pads are removed some functions may be tested only by the device manufacturer and not by the user. Mennitt teaches away from a device that may be tested by the user, since the test pads are gone by the time the device is in the user's hands. Having failed to teach or suggest each and every limitation of claim 2, the art referenced as

rendering dependent claim 2 obvious cannot serve as the basis for rejection. Therefore, claim 2 is allowable.

Applicants submit that claims 1 through 7 are clearly allowable over the cited prior art.

Applicants request the allowance of claims 1 through 7 and the case passed for issue.

Respectfully submitted,

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